REMARKS

Claims 1-30, all the claims pending in the application, stand rejected. Claims 1 and 18 are amended to include the features of claim 2. Claim 2 is cancelled. New claims 31-34 are added.

In response to Applicant's arguments filed 11/30/2007, the previous rejection has been withdrawn. However, a new ground(s) of rejection is made in view of Gu et al.

Claim Rejections - 35 USC § 102

Claims 1, 3, 4, 9, 11-14, 16, 18, 23, 26 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Gu et al. (5,920,084). This rejection is traversed for at least the following reasons.

Claims 1 and 18

The Examiner asserts that Gu et al. teaches all of the limitations of independent claims 1 and 18, including a source electrode and a drain electrode (see Fig. 6, source 31. drain 29); a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 6, semiconducting region 23); a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 6, gate electrode 17, inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device, g_m = dl / dE, where dl = change in drain current and dE = change in gate voltage); and an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes is greater than the shortest physical distance between the source and drain electrodes (see Fig. 6, insulating region 33, current path between source 31 and drain 29 must be larger than the physical separation distance between source 31 and drain 29).

The Examiner admits that the limitations of claim 2 are not taught in Gu et al. Thus, Applicants have amended product claim 1 and method claim 18 to expressly recite that "the length of the shortest current path through the semiconducting region between the source and

drain electrodes exceeds 1.05 times the shortest physical distance between the source and drain electrodes."

As demonstrated subsequently, not only is this feature absent from the teachings of Gu, it would not be obvious to implement the recited limitation on the basis of the teachings in Gu.

Claims 3, 4, 9, 11-14, 16, 23, 26

These claims, which depend from one of amended independent claims 1 and 18, would be patentable for at least the reasons given for parent claims 1 and 18, as detailed subsequently.

Claim 29

Claim 29 is rejected as being anticipated by Gu et al. However, claim 29 depends from claim 28, which the Examiner admits Gu et al does not anticipate. Thus, the rejection necessarily is overcome.

Claim Rejections - 35 USC § 103

Claims 2, 10, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al.. This rejection is traversed for at least the following reasons.

Claim 2

The Examiner admits that Gu et al. does not teach shortest current path through the semiconductor region between the source and drain to be greater than 1.05 times the shortest physical distance between the source and drain nor does it teach physical distance between the source and drain to be less than one micrometer.

The Examiner asserts that in the same field of endeavor, given the teaching of Gu, it would have been obvious to determine the optimum shortest current path or physical distance between the source and drain electrodes (citing *In re Aller, Lacey, and Hall* (10 USPQ 233-237)). The Examiner asserts that it is not inventive to discover optimum or workable ranges by routine experimentation, and that criticality has not been shown.

No Lengthened Shortest Current Path

Applicants respectfully submit that the Examiner's analysis on the basis of the teachings of Figure 6 of Gu, is unsupported by the disclosure of the reference. Applicants respectfully

refer the Examiner to the written description at col. 10, lines 54 to 58 in relation to the feature referenced in Figure 6. This section details that it is "inevitable" that a bit of the semiconductor layer 23 is etched along with the contact layer 25 which is above the semiconductor layer 23. Applicants respectfully submit that this does not constitute a positive teaching to provide a **lengthened** shortest current path, because the recess from which the lengthened shortest current path results is only described as an unavoidable result of the etching process used to pattern the contact layer 25.

Applicants respectfully submit that there is no teaching in Gu that (1) this recess would provide any positive effect on the properties of the transistor, or (2) the depth of the recess should be increased beyond that which is an unavoidable result of the use of an etching process for the pattering of the contact layer 25.

Claims 10 and 17

These claims would be patentable for the reasons given for amended parent claim 1.

Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to claim 1 above, and further in view of Hirai et al. (2003/0160235) This rejection is traversed for at least the following reasons.

The Examiner admits that Gu et al. does not teach a device as claimed in claim 1, wherein (1) the source and drain electrodes comprise a conducting polymer, (2) the semiconductor region comprises a solution processible conjugated polymeric or oligomeric material, and (3) the semiconducting region comprises a material of small conjugated molecules with solubilising side chains. The Examiner looks to Hirai et al. for these teachings, but does not rely on Hirai et al for a lengthened shortest current path.

The rejected claims would be patentable for the reasons given for amended parent claim 1.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to claim 1 above, and further in view of Kostantinos et al. (JP 2000-260999). This rejection is traversed for at least the following reasons.

The Examiner admits that Gu et al. does not teach a device as claimed in claim 1, wherein the semiconducting region comprises organic-inorganic hybrid materials self assembled from solution. The Examiner looks to Kostantinos et al. for such teaching but does not rely on Kostantinos et al for a lengthened shortest current path.

The rejected claims would be patentable for the reasons given for amended parent claim 1.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to claim 1 above, and further in view of Han et al. This rejection is traversed for at least the following reasons.

As previously noted, Hirai et al. does not teach a lengthened shortest current path. The rejected claims would be patentable for the reasons given for amended parent claim 1.

Claims 19, 20, 22, 24, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to claim 18 above, and further in view of Hirai et al. This rejection is traversed for at least the following reasons.

The Examiner looks to Hirai et al. for teachings related to limitations added by these dependent claim, but does not rely on Hirai et al for a lengthened shortest current path.

The rejected claims would be patentable for the reasons given for amended parent claim 18.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to claim 18 above. This rejection is traversed for at least the following reasons.

The rejected claims would be patentable for the reasons given for amended parent claim 18.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to claim 18 above, and further in view of Berger et al. This rejection is traversed for at least the following reasons.

The Examiner admits that Gu et al. does not teach a method as claimed in claim 18, wherein forming one or more components of the device using electron beam lithography. The

Examiner looks to Berger et al for such teaching but does not rely on Berger et al for a lengthened shortest current path.

The rejected claims would be patentable for the reasons given for amended parent claim 18.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to claim 18 above, and further in view of Grewell et al. This rejection is traversed for at least the following reasons.

The Examiner admits that Gu et al. does not teach a method as claimed in claim 18, wherein embossing techniques are used to forming the insulating region. The Examiner looks to Grewell et al for such teaching but does not rely on Grewell et al for a lengthened shortest current path.

The rejected claims would be patentable for the reasons given for amended parent claim 18.

Claim 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to claim 28 above, and further in view of Hirai et al. This rejection is traversed for at least the following reasons.

The Examiner admits that Gu et al. does not teach a method as claimed in claim 18, wherein insulating material is deposited from a vapor phase. The Examiner looks to Hirai et al for such teaching but does not rely on Hirai et al for a lengthened shortest current path.

The rejected claims would be patentable for the reasons given for amended parent claims 18 and 28.

New Claims

Applicants have added four new independent claims that are directed to novel and unobvious features of the originally disclosed invention that are not taught in Gu or other prior art references.

New independent claims 31 and 33 specify that the increase in length of the shortest current path is done for the purpose of suppressing the off-current of the electronic switching

device. There is no teaching in Gu to etch the semiconductor layer of Figure 6 for any positive purpose, and more specifically, not for the purpose recited in these two claims.

New independent claims 32 and 34 specify that the shortest current path through the semiconducting region is defined other than by etching. Gu only describes the etching of the semiconductor layer as an inevitable result of the etching process. There is no teaching in Gu of any beneficial feature of the etching of the semiconductor layer 23. Moreover, there is no teaching or suggestion in Gu to take steps to similarly remove part of the semiconductor layer 23 in the case of patterning the contact layer 25 by a technique other than the etching technique used in Gu.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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